IDEC Chip Design Contest

# Design of 24GHz Frequency Synthesizer

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- This research describes a 24 GHz frequency synthesizer (FS) for automotive collision avoidance radar.
- The voltage-controlled oscillator (VCO) is designed in modified current-reuse configuration, where transistors are biased in subthreshold region to save power consumption.
- The proposed FS showed low power consumption of 3.52mWwith the supply voltage of 0.9 V.
- The designed FS has  a low phase noise of −116.2 dBc @1 MHz and −124.1 dBc @10 MHz.
- The settling time of designed FS is 3.1ns.
- The FS has very low peak-to-peak jitter noise of 3.5 ps, and very low rms jitter of 0.75 ps.


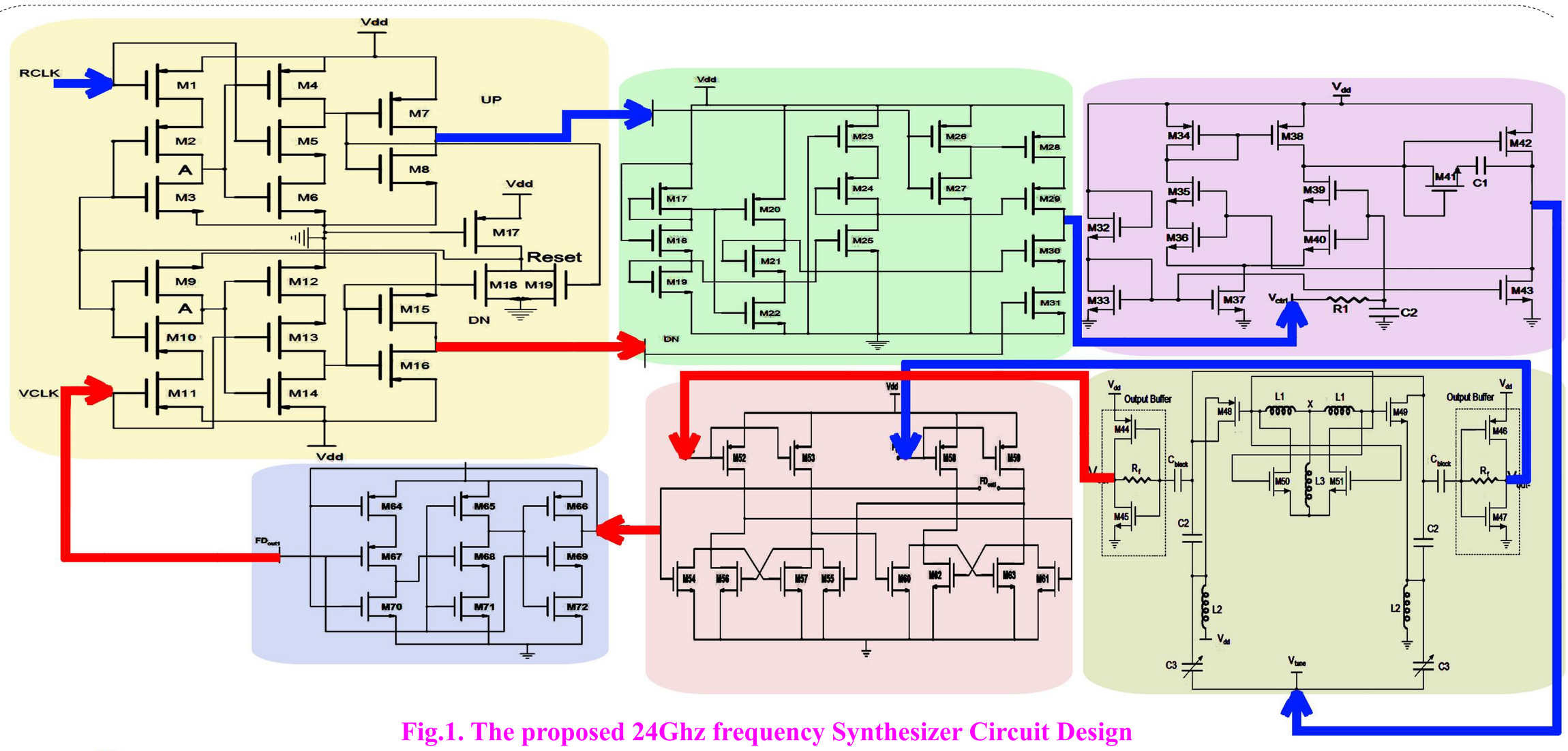


Fig.1. The proposed 24Ghz frequency Synthesizer Circuit Design

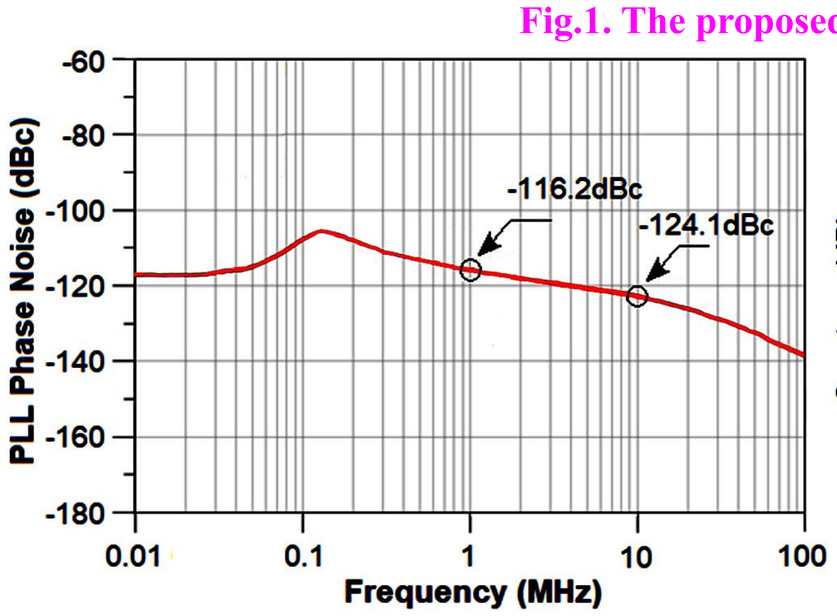


Fig.2. Close-poop PLL phase noise

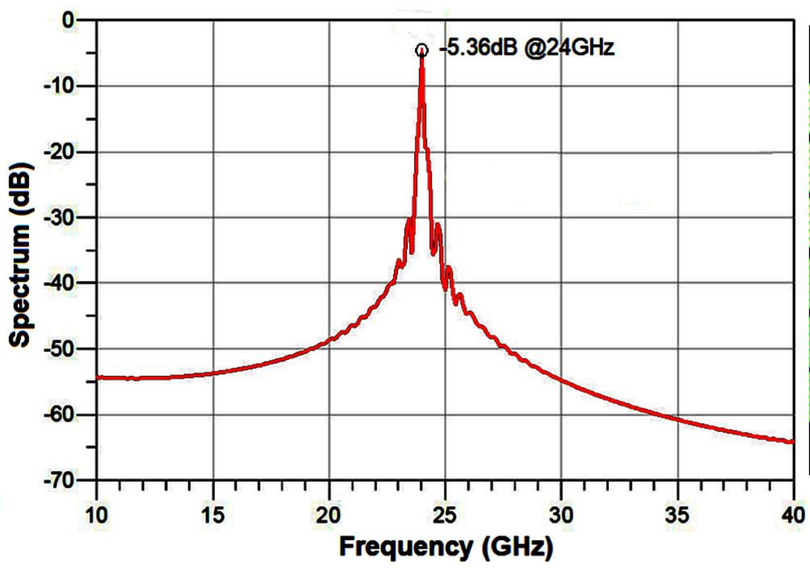


Fig.3. Closed-loop spectrum

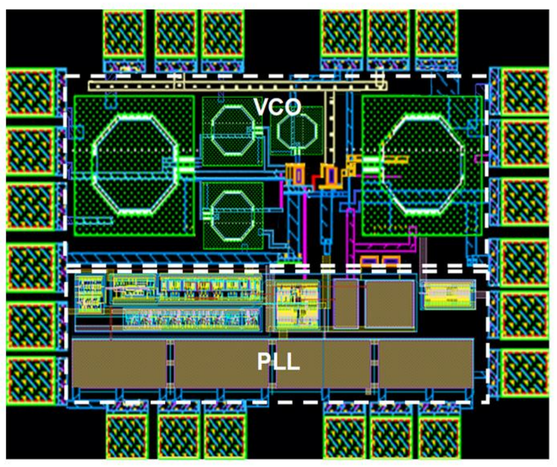


Fig.4. Dielayout

- A fully integrated low-power and low-phase noise FS with operating frequency of 24-GHz for ACAR applications is presented.
- The VCO achieved a FOM of −199.7 dB using current reuse and negative resistance technique.
- The designed VCO has low phase noise of −104.32 dBc @1 MHz and 127.02 dBc @10 MHz.
- The VCO has wide oscillator frequency range of 7.5% at the frequency range of 24–25.8 GHz.
- The size of the die of designed FS is 0.776 × 0.776 $mm^2$ including pads.

※ The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.